Deep Submicron VLSI Design

Silicon-on-Insulator Circuit Design
Outline

• Overview of Silicon-on-Insulator (SOI)
• Floating Body Voltage
• SOI Advantages
• SOI Disadvantages
• Implications for Circuit Styles
• Summary

Material from: CMOS VLSI Design
By Neil E. Weste and David Harris
SOI Overview

• Adopted for IBM PowerPC μprocessors in 1998
  – Higher performance and lower power than CMOS
  – Higher cost and complicated circuit design

• Differences from bulk CMOS:
  – Transistor source, drain, & body surrounded by insulating SiO₂ rather than substrate (well)
  – Eliminates most diffusion parasitic C
  – Body no longer tied to GND or $V_{DD}$
    • Any change in body voltage modulates $V_t$
SOI Inverter

Diagram showing a SOI Inverter with labels for GND, V_{DD}, nMOS Transistor, pMOS Transistor, p-substrate, and Insulator.
Two Types of SOI

- **Partially depleted (PD)**
  - Body thicker than channel depletion width
  - Body voltage changes
  - Depending on charge injected into bulk
  - Causes *history effect*, which changes $V_t$

- **Fully depleted (FD)**
  - Body thinner than channel depletion width
  - Fixed body charge
  - Body voltage does not change
  - Thin body makes this very hard to manufacture
  - Therefore, not used
IBM SOI Process
Floating Body Voltage

- Body voltage varies as body charges/discharges

- Charge paths to/from floating body
Body Charge Paths

- Reverse-biased drain-to-body $D_{db}$ and source-to-body $D_{sb}$ junctions
  - Carry small diode leakage currents into body
- High-energy carriers cause impact ionization
  - Create $e^-$ hole pairs
    - Injected into gate or gate oxide
    - Cause hot $e^-$ wearout
    - Corresponding holes accumulate in body
  - Most pronounced at $V_{DS} >$ intended operating point
  - $I_{ii}$ is impaction ionization current into body
Ways for Charge to Exit Body

- As body voltage increases
  - Source-to-body $D_{sb}$ junction slightly forward biases
  - Charge exiting from $D_{sb}$ balances charge entering from $D_{db}$
- Rising gate/drain capacitively couples body upward
  - May strongly forward-bias source-to-body $D_{sb}$ junction and spill charge out of body
  - During long idle periods body $V$ goes to equilibrium
  - When switching resumes
    - Charge spills of body
    - Shifts body voltage and $V_t$ significantly
SOI Advantages

- Lower $C_{diffusion}$ – largely eliminated
- Lower parasitic delay
- Lower dynamic power consumption
- Potential for lower $V_t$
  - Bulk CMOS – $V_t$ varies with channel length
    - Poly etching variations cause $V_t$ variations
    - Must make $V_t$ high enough to limit worst-case subthreshold leakage
  - SOI
    - Smaller threshold variations
    - Nominal $V_t$ can be close to worst-case
    - Faster transistors, especially at low $V_{DD}$
Subthreshold Swing

• Bulk CMOS – subthreshold slope of $n \nu_T \ln 10$
  – $\nu_T = kT/q$, $n$ is process dependent
• Bulk CMOS has $n = 1.5$, subthreshold slope of 90 mV/decade
  – For each 90 mV decrease in $V_{gs}$ below $V_t$
    subthreshold $I$ reduces 10 X
• SOI (IBM) -- subthreshold slope of 75-85 mV/decade
• Double-gate MOSFETs and FINFETs are SOI variations
  – Offer even lower subthreshold slopes
  – Gate surrounds channel – turns off quicker
Latchup

- SOI is immune to latchup
SOI Disadvantages

- **History effect**
  - Changes in body $V$ modulate $V_t$, vary gate delay
- Body voltage depends on whether device was idle or switching -- Delay is $f$ (switching history)
- Overall, elevated body voltage:
  - Reduces $V_t$ and makes gates faster
- Model history effect
  - Assign different propagation and contamination delays to each gate
  - IBM – history effect causes 8% gate delay variation
    - Less than process variations
More Disadvantages

• History effect:
  – Causes significant mismatches between otherwise matched transistors
    • Sense amplifier
    • Analog OPAMP
    • Gilbert cell analog multiplier (mixer)
  – Solve by introducing substrate contact to make transistor pair behave identically
Parasitic Bipolar Transistor

- Problem because body/base floats
Current Pulse Problems

• Hold source & drain high for a long time
  – While gate is low
  – Base floats high through diode leakage
• Then pull source low, and \( npn \) transistor turns ON
  – \( I_B \) flows from body/base to source/emitter
  – Causes \( \beta I_B \) to flow from drain/collector to source/emitter
    • \( \beta \) depends on channel length & doping but > 1
  – Get a current pulse from drain to source even though transistor should be OFF
Current Pulse

• Called *Pass-gate Leakage*
• Often happens to OFF pass transistors where source & drain are initially high and then go low
  – No problem for static circuits
    • ON transistors oppose glitch
  – Causes malfunctions in dynamic latches in logic
    • Need strong keepers to hold node steady
Self-Heating Problem

- SiO$_2$ is great thermal and electrical insulator
  - Heat accumulates in transistors
  - Rather than spreading to substrate as in CMOS
- Individual transistors with large power
  - Heat substantially more than the die
  - Deliver less current, slower
- Can raise $T$ by 10 to 15 °C for clock and I/O devices
  - Less significant for logic
Implication for Circuits

• SOI good for fast CMOS logic
  – Smaller $C_{\text{diffusion}}$ gives lower parasitic delay
  – Lower $V_t$ gives better drive current and lower delay
• SOI attractive for low-power design
  – Smaller $C_{\text{diffusion}}$ reduces dynamic power
  – Easier to scale down $V_{DD}$
  – Consider FINFETs – sharper subthreshold slope
• Static CMOS in PD SOI
  – Similar to bulk CMOS family, but faster
  – History effect causes pattern dependent delay variation
Dynamic Gates

- New Problem – pass-gate leakage
  - Causes dynamic latches and gates to lose charge on dynamic node

![Diagram of dynamic gate leakage](image)
Solve Pass-gate Leakage

• Staticize capacitive storage nodes
  – Cross-coupled inverter pair for latches
• \textit{p}MOS keeper for dynamic gates
  – Can pre-discharge internal nodes to prevent pass-gate leakage
    • Then have a charge sharing problem on internal nodes
• Staticizing transistors must be $\frac{1}{4}$ as strong as normal path
  – Slow down gates
Gated Clock Problems

• Gated clocks have increased skew
  – History effect makes clock switch more slowly
    • When activated after being disabled for a long time
SOI RAMs

• Require elaborate design
  – Pass-gate leakage
  – Floating bodies
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